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DESIGN AND IMPLEMENTATION OF SAMPLING RATE CONVERSION SYSTEM FOR ELECTROENCEPHALOGRAM (EEG) ON FPGA DEVICE

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ABSTRACT

The wide scale use of digital communication and digital media have made the necessity of methods to process digital data more important now-a-days. The signal-rate system with digital signal processing has evolved the key of fastest speed of digital signal processor. Field Programmable Gate Array **(***FPGA***)** *offers the best solution for addressing the needs of high performance DSP systems. The focus of this paper is on Sampling Rate Conversion (SRC) and DSP functions, namely filtering signals to remove unwanted frequency. This concept leads to a chip with attractive features like, low requirements for the coefficient word lengths, significant saving in computation and storage requirements results in a significant reduction in its dynamic power consumption. This paper introduces an efficient FPGA realization of multi rate decimation filter with a narrow pass - band and a narrow transition band to reduce the frequency sample rate by factor L/M which is applied to generate the bio-signal like EEG signals.*

KEYWORDS: *Bio-Chip, Multi-Rate, Decimate, Interpolate, EEG*

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